Core Switch Debugging Cable Selection

AI Overview

Selecting the correct debug cable depends on the processor architecture, supported debug protocols, and the multicore configuration of your target system.Key Considerations for Cable Selection1. Identify the Debug Protocol: Most modern cores, including Infineon TriCore and AURIX families, support JTAG and DAP protocols. JTAG is a synchronous serial protocol that allows multiple devices to be chained, but some cores (e.g., Cerberus IO Client devices) have restrictions on daisy-chaining, requiring careful placement in the chain . Ensure your target processor supports the protocol your debugger uses. 2. Match the Connector Type: Debug cables come with various connectors. Check the target board's debug port and select a cable or adapter that matches the pinout and signal requirements. Lauterbach provides detailed connector standards and signal descriptions for TriCore devices . 3. Multicore Debugging Requirements: For multicore processors, such as dual-core SPC56x or AURIX devices, a single debug cable can often control multiple cores if it has the necessary licenses . TRACE32 allows configuration of each core via commands like SYStem.CONFIG.CORE to assign the debugger to the correct core. Ensure the cable supports the required frequency and bandwidth for all cores simultaneously. 4. Cable Quality and Signal Integrity: High-speed debug interfaces require cables with low capacitance and proper shielding to prevent signal degradation. For longer distances or high-frequency JTAG, consider cables specifically rated for your target frequency . 5. Practical Connection Steps:Power off the target before connecting the cable.Connect the host system, debugger hardware, and debug cable.Power on the debugger hardware, then the target.Configure the debugger via startup scripts or TRACE32 settings .Disconnect in reverse order to avoid damage. 6. Licensing and Features: Some debug cables include licenses for multicore debugging or advanced trace features. Verify that your cable supports all cores and trace capabilities required for...

Article Content

Lauterbach multicore debugging guide

3.1 Dual-core debug environment There is a possibility to debug dual-core processor with single TRACE32 PowerView window, but for better orientation and easier debugging there is the possibility

STM32H7x5/x7 dual-core microcontroller debugging

STM32H7x5/x7 dual-core microcontroller debugging The STM32H7x5/x7 dual-core microcontroller lines as described in Table 1. Applicable products (named STM32H7x5/x7 microcontrollers in this

Introduction | ModusToolbox™ ecosystem documentation

ModusToolbox™ software is a collection of GUI and non-GUI tools, libraries, and programs used to develop embedded applications. Desktop tools are installed as part of the

STM32 Nucleo-64 boards (MB1717)

Introduction The STM32 Nucleo-64 boards, based on the MB1717 reference board (NUCLEO-C031C6 and NUCLEO-C051C8 order codes) provide an affordable and flexible way for users to try out new

Hardware Debugging

Hardware Debugging Introduction In this lab you will use the uart_led design that was introduced in the previous labs. You will use Mark Debug feature and also the available Integrated Logic Analyzer

core switch -selection

Finally, look at "core switches", like the 9600. 9600 is aimed at core switching because the line cards are specifically designed for that specific role. People have known to directly connect

Hardware/Software Debugging

Hardware/Software Debugging Introduction This lab is a continuation of the previous RTL Kernel Wizard Lab lab. You will use ChipScope to monitor signals at the kernel interface level and perform software

MITO8M-AN-001: Advanced multicore debugging, tracing, and energy

The following sections describe how to configure the Lauterbach TRACE32® debugger to support debug and trace of Linux running on the quad-core i 8M Application Processor by NXP Semiconductors.

STM32 Nucleo-64 boards (MB1136)

For information about debugging and programming features, refer to the user manual ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32 (UM1075), which describes in detail all the ST

TriCore Debugger and Trace

The command CORE.select allows to switch between cores (also visible and changeable via the “Status Bar” (ide_user.pdf)). Many commands also offer the option /CORE <core>, e.g.:

Lauterbach multicore debugging guide

If the target provides a joint debug interface for several cores it is necessary to inform the TRACE32 instance which core it controls for debugging. The command SYStem NFIG RE allows to

A Practical Guide To Cable Selection

Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI''s terms and conditions of sale

A Software Guide to Universal Debug Engine

Connect the Debug Extender with your target by the 14-wire, 16-wire or 20-wire JTAG cable. Refer to the appendix Hardware Description of the user''s manual for more information about the correct pin

ARMv8-A/-R Debugger

Usually the access ports, the core debug base and the CTI base are set when the CPU/SoC is selected, so the following SYStem NFIG commands would not be required.

New Concepts for Multicore Debugging

Control of several cores over a common debug interface This new concept means that only one PowerDebug Module and one debug cable are required to debug all cores in a SoC. For this to work,

A Software Guide to Universal Debug Engine

Multi-Core Debugging Example with AURIX TC2xx Understanding a Multi-Core Configuration Creating a New Workspace Preparing the Debugger Show, Hide and Group Windows-Related Perspectives

Introduction to debug toolbox for STM32 MCUs

Introduction STM32 end-users are sometimes confronted with non- or partially-functional systems during product development. The best approach to use for the debug process is not always obvious,

Application Note Debug Cable TriCore

It depends on the TriCore device, the debug cable and the debug connector which debug protocol can be
 used by the debugger to communicate with the device.

TriCore Debugger and Trace

The Debug Cable comes with a license for debugging. Detailed information is available in chapter “Debug Cables and CombiProbe Whiskers” in Application Note Debug Cable TriCore, page 22

What is Core Switch and How to Choose

Discover what a core switch is and learn how to choose the right one for your network. Explore key features in selecting a core layer switch. Make

Serial Console

Special Login Special login can be used to access another device (like a switch, for example) that is connected through a serial cable by opening a telnet/ssh session that will get you

ARM JTAG Interface Specifications

You can identify the debug cable version by typing ”version.hardware” into the TRACE32 command line or compare your debug cable with the pictures below. Debug cable versions and a description of the

AN80994 Design Considerations for Electrical Fast Transient (EFT)

With the use of switching-power supplies, power controllers can be susceptible to noise. This section provides considerations for power supply schematic and layout design for transient immunity.

Diving into JTAG — Debugging (Part 2)

As noted in my previous article Diving into JTAG protocol. Part 1 — Overview, JTAG was initially developed for testing integrated circuits and printed

Problem with Core switch and distribution switches

we have core switch 3750 connect with 14 distribution switches 2960 with 2 uplink each, 3 switch work on speed 100 when i change one to 1000 i notice a strange behavoir in the enviroment

Contact Us

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